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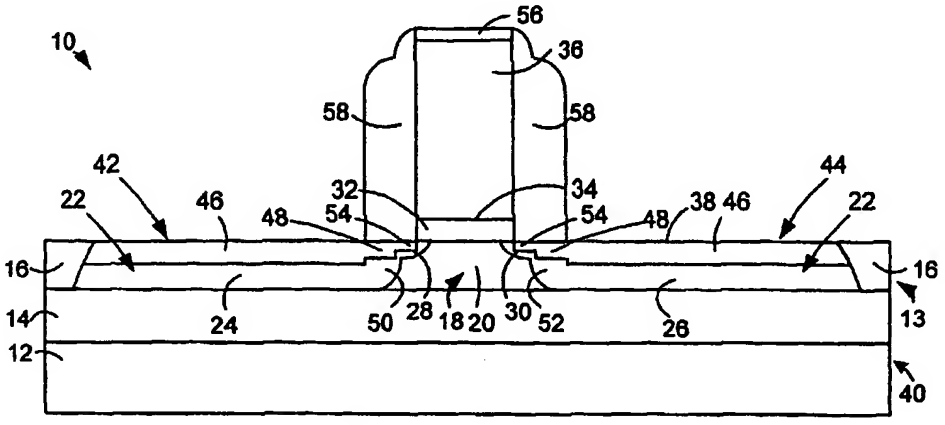

(57) Abstract: A transistor device (10) formed on a semiconductor substrate (12) with an active layer (13) disposed on the semiconductor substrate having active regions (18) defined by isolation trenches (16). The device includes a gate (36) defining a channel (20) interposed between a source and a drain (22) formed within the active region of the substrate. Further, the device includes a multi-thickness silicide layer (42 and 44) formed on the main source and drain regions (24 and 26) and source and drain extension regions (28 and 30) wherein a portion (54) of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion (46) of the silicide layer which is formed on the mainn source and drain regions. The device further includes a second thin silicide layer formed on a polysilicon electrode of the gate. Further still, the device includes a disposable spacer used in the formation of the device. Further, the device includes a plurality of thin silicide layers formed on the source and the drain. Additionally, at least an upper silicide layer of the plurality of thin silicide layers extends beyond a lower silicide layer. Further still, the device includes a plurality of spacers used in the formation of the device. The device further includes a second plurality of thin silicide layers formed on a polysilicon electrode of the gate.

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For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

MULTI-THICKNESS SILICIDE DEVICE

TECHNICAL FIELD

The present invention generally relates to the manufacture of semiconductor devices and, more specifically, relates to the manufacture of devices including multi-thickness silicide, multi-layered silicide and multi-thickness multi-layered silicide.

BACKGROUND ART

Integrated electrical circuit devices such as electrically erasable programmable read only memories (EEPROMs), transistors, diodes, thyristers and the like are usually manufactured on a semiconductor substrate, such as silicon. Such semiconductor substrates, even when doped, are usually more resistive than most metal-containing materials. Resistive contacts and interconnects are not desirable for electrical circuits due to the fact that resistance limits maximum current flow, may create heat, and may result in reduced circuit accuracy, consistency, and performance. Therefore, devices such as metal oxide semiconductor (MOS) transistors typically use a silicide or salicide layer over the source, drain and gate regions in order to reduce contact resistance. However, such transistors with silicide or salicide layers still tend to suffer from high contact resistance.

Transistors made on silicon-on-insulator (SOI) structures suffer from what is referred to as floating body effect (FBE) in addition to the above disadvantages. The FBE is when a body region voltage varies undesirably because the body region is electrically isolated from the substrate. The FBE introduces several undesirable characteristics. FBE causes, for example, sharp increases in the relationship between drain current and drain voltage ("kink effect"), anomalous subthreshold current, transient current overshoot, and early device voltage V_{DS} breakdown. The kink effect may lead to lower device gain, which is undesirable in analog applications. The FBE remains a major obstacle to acceptable operation of SOI MOSFET transistors.

U.S. Patent No. 5,352,631addresses the above discussed disadvantages relating to contact resistance. In particular, U.S. Patent No. 5,352,631 describes a method of forming one silicide species overlying the gate region, and another silicide species overlying the source and drain regions. However, there is no suggestion as to how to overcome the resistance associated with lightly doped drain and source regions (also referred to herein as source and drain extension regions). Further, there is no suggestion as to how to overcome the disadvantages due to the FBE.

In U.S. Patent No. 5,965,917, one suggestion to overcome some of the disadvantages due to the FBE is to include a metal connector (electrical contact) that directly contacts a top silicide region, a side of a first doped region and a side of a body region. The disclosed device overcomes some of the disadvantages due to the FBE. For example, a voltage applied to the electrical contact sets the voltage of the body region because the electrical contact is directly coupled to the body region. However, there is no suggestion as to how to overcome the resistance in the lightly doped drain and source extension regions.

Therefore, there exists a need in the art for an electrical device which tailors resistance in the various regions such as the polysilicon regions of the source and drain regions, the junction regions of the source and drain regions, and the source and the drain extension regions. Further, there is a need in the art for an electrical

device which, in addition to providing tailored resistance, also reduces the disadvantages due to the FBE associated with such devices on SOI structures.

DISCLOSURE OF THE INVENTION

According to one aspect of the invention, the invention is a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The device includes a gate defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate. The source and the drain include a main source and drain region as well as source and drain extension regions. Further, the device includes a multi-thickness silicide layer formed on the main source and drain and the source and drain extension regions. Additionally, a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the multi-thickness silicide layer which is formed on the main source and drain regions.

According to one aspect of the invention, the invention is a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The device includes a gate defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate. Further, the device includes a plurality of thin silicide layers formed on the source and the drain. Additionally, at least an upper silicide layer of the plurality of thin silicide layers extends beyond a lower silicide layer. The device also includes a plurality of spacers used in the formation of the device.

According to one aspect of the invention, the invention is a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The device includes a gate defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate. Further, the device includes a plurality of thin silicide layers formed on the source and the drain. Additionally, at least an upper silicide layer of the plurality of thin silicide layers extends beyond a lower silicide layer. The device also includes a disposable spacer used in the formation of the device.

According to another aspect of the invention, the plurality of spacers are permanent spacers formed in successive steps during a formation process of the device.

According to another aspect of the invention, a first intermediate spacer is formed from the disposable spacer to control the formation of the source and drain and multi-thickness silicide layer.

According to another aspect of the invention, the multi-thickness silicide layer includes at least two layers of silicide of different species.

According to another aspect of the invention, the semiconductor substrate is a semiconductor-on-insulator (SOI) substrate with a buried oxide (BOX) layer interposed between the active layer and a main semiconductor substrate and wherein the BOX layer further defines the active regions.

According to another aspect of the invention, the semiconductor substrate is on a germanium-on-insulator (GOI) substrate.

According to another aspect of the invention, the invention is a method of fabricating a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The method includes the step of forming a gate defining a channel interposed between a source and a drain formed within an active region of the semiconductor substrate. Further, the method includes forming a multi-thickness silicide layer on

the main source and drain and the source and drain extension regions. Additionally, a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the multi-thickness silicide layer which is formed on the main source and drain regions.

According to another aspect of the invention, the invention is a method of fabricating a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The method includes the step of forming a gate defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate. Further, the method includes forming a plurality of thin silicide layers on the source and the drain. Further, the method includes the step of forming a first plurality of spacers on the gate side walls. In addition, the method includes the step of forming a second plurality of spacers on the first plurality of spacers. Additionally, at least an upper silicide layer of the plurality of thin silicide layers extends beyond a lower silicide layer.

According to another aspect of the invention, the invention is a method of fabricating a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches. The method includes the step of forming a gate defining a channel interposed between a source and a drain formed within the active region of the semiconductor substrate. Further, the method includes forming a plurality of thin silicide layers on the source and the drain. Further, the method includes the step of forming a disposable spacer on a side wall of the gate. Additionally, at least an upper silicide layer of the plurality of thin silicide layers extends beyond a lower silicide layer.

According to another aspect of the method, the method includes the additional step of etching selectively the disposable spacer in stages in order to tailor the formation of the multi-thickness silicide layers.

According to another aspect of the method, the semiconductor substrate is a semiconductor-on-insulator (SOI) substrate with a buried oxide (BOX) layer interposed between the active layer and a main semiconductor substrate and wherein the active regions are further defined by the BOX layer.

BRIEF DESCRIPTION OF DRAWINGS

These and further features of the present invention will be apparent with reference to the following description and drawings, wherein:

FIG. 1 is a cross-section of an SOI transistor device including multi-thickness silicide layers according to the present invention;

FIGS. 2 - 6 are cross-section views of the SOI transistor device of FIG. 1 including multi-thickness silicide layers according to the present invention at intermediate stages of manufacture;

FIG. 7 is a flow diagram of a method of manufacturing the SOI transistor device of FIG. 1 including multi-thickness silicide layers according to the present invention;

FIG. 8 is a cross-section of an SOI transistor device including multi-thickness silicide layers according to another embodiment of the present invention;

FIGS. 9 - 14 are cross-section views of the SOI transistor device of FIG. 8 including multi-thickness silicide layers according to the present invention at intermediate stages of manufacture;

FIG. 15 is a flow diagram of a method of manufacturing the SOI transistor device of FIG. 8 including multi-thickness silicide layers according to the present invention;

FIG. 16 is a cross-section of an SOI transistor device including multi-thickness silicide layers according to another embodiment of the present invention;

FIGS. 17 – 22 are cross-section views of the SOI transistor device of FIG. 16 including multi-thickness silicide layers according to the present invention at intermediate stages of manufacture; and

FIG. 23 is a flow diagram of a method of manufacturing the SOI transistor device of FIG. 16 including multi-thickness silicide layers according to the present invention.

MODE(S) FOR CARRYING OUT THE INVENTION

In the detailed description that follows, identical components have been given the same reference numerals. To illustrate the present invention in a clear and concise manner, the drawings may not necessarily be to scale and certain features may be shown in a partial schematic format.

An SOI transistor device including multi-thickness silicide layers will now be described in accordance with the present invention. The device includes a gate defining a channel interposed between a source and a drain and is disposed within one of the active regions of an SOI structure. Further, the device includes a multi-thickness silicide layer formed on the main source and drain regions and the source and drain extension regions as will be described in more detail below. Additionally, a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the multi-thickness silicide layer which is formed on the main source and drain regions. The device may include a further silicide layer formed on a polysilicon electrode of the gate. Further still, the multi-thickness silicide layers may include at least two layers of silicide of two different species.

The SOI transistor device including multi-thickness silicide layers results in an SOI transistor device with significantly reduced contact resistance in the main source/drain regions compared with conventional transistor devices. Additionally, the SOI transistor device including multi-thickness silicide layers and a silicide layer on the polysilicon gate electrode helps reduce AC effects. Further, the very thin silicide layer formed on the source/drain extension regions helps to reduce the FBE within the SOI structure.

Referring initially to FIG. 1, an SOI transistor device of the present invention is shown generally designated as 10. The SOI transistor device 10 is formed within a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 12, a buried oxide (BOX) layer 14 formed on the semiconductor substrate 12, and a semiconductor layer 13 disposed on the BOX layer 14. Within the semiconductor layer 13, shallow trench isolation (STI) regions 16 define a semiconductor active region 18 of which one is shown in FIG. 1.

In an exemplary embodiment, as illustrated in FIG. 1, the active region 18 has a p-type region, or channel 20, and two N+ (source and drain) regions 22. The channel 20 is interposed between the source and drain regions 22. Alternatively, an n-type channel could be interposed between two P+ regions as will be readily appreciated. The source and drain regions 22 include respective deep implant regions 24 and 26, as well as respective extension regions 28 and 30. A gate dielectric 32 is interposed between a lower surface 34 of a gate electrode 36 and an upper surface 38 of the SOI semiconductor substrate 40. The gate dielectric 32 illustrated in FIG. 1 is a single layer dielectric, however the gate dielectric could be a multi-layer dielectric.

Multi-thickness silicide layers 42, 44 are disposed on a portion of the two source and drain regions 22. Silicide regions 46 are formed on the polysilicon regions of the respective deep implant regions 24 and 26.

Thinner silicide regions 48 are formed over the respective deep implant junction regions 50 and 52. Very thin silicide regions 54 are formed over the respective extension regions 28 and 30. The multi-thickness silicide layers 42, 44 may be made of typical, well-known silicides, such as cobalt silicide ($CoSi_2$), titanium silicide ($TiSi_2$), tantalum silicide ($TaSi_2$), nickel silicide ($NiSi_2$) or the like. In an exemplary embodiment, the multi-thickness silicide layers 42, 44 are of $CoSi_2$. Silicide regions 46 could have a thickness of between 100 Å (angstroms) and 300 Å. Silicide regions 48 could have a thickness of between 50 Å and 250 Å. Very thin silicide regions 54 could have a thickness of between 25 Å and 100 Å.

On top of the gate electrode 36 is a silicide layer 56. The silicide layer 56 may be made of the same suitable silicide materials described above. The silicide layer 56 may be made of the same material as the silicide layers 42, 44 or may be made of another silicide material described above. An exemplary silicide layer 56 may have a thickness of between 100 Å and 200 Å.

It will be appreciated that the active region 18, the channel 20, the source and drain regions 22, the gate dielectric 32, the gate electrode 36, the silicide layer 56, and the multi-thickness silicide layers 42, 44, together form the SOI transistor device of the present invention. The principles of operation of an SOI transistor having multi-thickness silicide layers over the source and the drain regions of the gate device will be further explained below. It will be appreciated that the SOI transistor device 10 may alternatively have other shapes than the shape shown in FIG. 1.

Spacers 58 extend upward from the upper surface 38 of the SOI substrate 40 on either side of the gate dielectric 32 and gate electrode 36. Although spacers 58 are shown, it should be understood that spacers are not required. The spacers 58 as shown may be used in formation of the multi-thickness layers 42, 44, which will further be described below.

The steps of a method 710 for fabricating a semiconductor device 210 (which may be similar to the semiconductor device 10 described above) are outlined in the flow chart shown in FIG. 7. FIGS. 2 - 6 illustrate various steps of the method 710. It will be appreciated that the method 710 and the semiconductor device 210 described below are merely exemplary, and that suitable embodiments of the many above-described variations in materials, thicknesses, and/or structures may alternatively be used in the method 710 and/or the semiconductor device 210.

In step 712, a conventional polysilicon gate is formed on an SOI substrate as an intermediate stage of manufacture for the SOI transistor device 210. As shown in FIG. 2, the SOI transistor device 210 includes a semiconductor substrate 212, a BOX layer 214 formed on the semiconductor substrate 212 and a semiconductor layer 213 disposed on the BOX layer 214. An exemplary BOX layer may have a thickness of between 1800 Å and 2200 Å. Whereas, an exemplary semiconductor layer 213 disposed on the BOX layer 214 may have a thickness of between 800 Å and 1000 Å. Suitable semiconductor materials such as silicon, carbide, germanium or the like may be used as the semiconductor layer 213 disposed on the BOX layer 214. Within the semiconductor layer 213 disposed on the BOX layer 214, are shallow trench isolation (STI) regions 216 which along with the BOX layer 214 define the location of a semiconductor active region for a future step. The STI regions 216 are insulator-filled to electrically isolate individual electrical devices such as the SOI transistor

device 210. Other isolation techniques that are known in the art may be used to isolate the SOI transistor device 210.

A gate dielectric 232 is interposed between the lower surface 234 of a gate electrode 236 and an upper surface 238 of a portion of the SOI semiconductor substrate 240. The gate dielectric 232 illustrated in FIG. 2 is a single-layer dielectric, however the gate dielectric could be a multi-layer dielectric as described above. The gate dielectric 232 may be made of suitable gate dielectric materials, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), silicon oxynitride (SiNO) or the like. In this embodiment, dielectric layer 232 is made of Si_3N_4. The exemplary dielectric layer 232 of Si_3N_4 may have a thickness of between 13 Å and 16 Å. The gate electrode 236 may be made of typical, well-known conductive materials, for example polysilicon. An exemplary gate electrode 236 may have a thickness of between 800 Å and 1200 Å.

In step 714, the source and drain regions 222 are formed as shown in FIG. 3. Prior to the source and drain formation, the semiconductor layer 213 of semiconductor substrate 240 may be appropriately doped to form a region or layer of electrically-active material for eventual use as an active region of the SOI transistor device 210 to be formed. For instance, boron or indium may be implanted to form a p-type region or channel for an n-type device and phosphorous or arsenic may be implanted to form an n-type region or channel for a p-type device. It should be understood that the semiconductor layer 213 could be appropriately doped prior to gate formation.

A more detailed description of an implantation process which will create the source and drain regions 222 which may be performed after the gate formation, is described below. In this exemplary embodiment, the channel region 220 underneath the gate dielectric 232, interposed between the source and the drain regions 222 is p-type doped prior to this step by either alternative described above.

Next, a disposable spacer may be formed over the gate to protect the gate electrode 236 and future extension regions 228, 230 from dopants used in the formation of the main source and the drain regions 226, 228. In order to form the disposable space, a spacer material such as an oxide material, for example silicon dioxide (SiO_2), silicon nitride (Si_3N_4) or the like, is then deposited on the substrate 240 (not shown). The deposition produces an oxide layer upon a top surface 238 of the SOI substrate 240. The oxide deposition may be performed, for example, by plasma enhanced chemical vapor deposition (PECVD).

The oxide is etched with a suitable etchant. The substrate oxide layers are reduced in size, leaving oxide spacers similar to spacers 268 shown in FIG. 5. The oxide spacers may extend from a surface 238 of the semiconductor substrate 240 to a height of between 3000 Å and 4000 Å.

Now, the main source and drain regions may be formed by a main perpendicular implant, which will not affect the extension implant regions due to the spacers acting as masks. The main perpendicular implant is a relatively high energy, high concentration implant which is capable of producing the source and drain deep implant regions 224 and 226. An exemplary range of concentration of these dopants is between $1X10^{18}$ and $1X10^{18}$ atoms/cm^3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm^2. The main perpendicular implants may be of the same material or may alternatively include different materials.

Then the disposable oxide spacers are etched with a suitable etchant and completely removed from the surface 238.

After formation of the main source and drain regions 224, 226, the lightly doped source and drain extension regions 228, 230 may be formed using techniques well known in the art for forming such extension layers. An extension perpendicular implant is a relatively low energy, low concentration implant which is capable of producing the source and drain extensions 228 and 230. The total concentration of the extension implants may be, for example, between $1X10^{18}$ atoms/cm^3 and $1X10^{18}$ atoms/cm^3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm^2. The extension perpendicular implants may be of the same material as the main perpendicular implant, or may alternatively include different materials. It should also be appreciated that the extension implants may be different from one another, if so desired. Thus, the main source and drain regions 222 are formed.

It will be appreciated that many alternative sequences or steps may be used to accomplish the implantation. For example, the perpendicular extension implants may be formed first and the spacers formed afterwards using the technique described above to protect the extension region material during the doping of the main source and drain regions 224, 226 using the perpendicular implant process described above. Additionally, although the extension implantation and the main implantation are illustrated as each involving one implant, it will be appreciated that a greater number of implants may be employed. Further, halo implants may be used in forming the extension implantation after gate 236 patterning or/and spacer 278 formation. For example, tilt angle extension implants (35-45 degrees) implanting In or BF_2 utilizing four rotations for a total implantation dose between $3.5X10^{13}$ and $5X10^{13}$ atoms/cm2 with energies 30-80 keV.

After implantation, the semiconductor device 210 may be subjected to rapid thermal annealing (RTA) at this time or at a later time. Exemplary RTA may be performed for between five and fifteen seconds at a temperature of 1,020 - 1,050°C.

Thereafter, in step 716, a metal layer 260 is formed overlying the source extension and drain extensions 228, 230 as well as the main source and drain regions 224, 226. The metal layer 260 is formed by one of either sputtering, chemical vapor deposition (CVD), or evaporation. The metal layer 260 may comprise any metal such as platinum, titanium, tantalum, nickel, cobalt, tungsten, and/or the like. In an exemplary embodiment, cobalt is used to form metal layer 260. Cobalt is preferred due to the fact that cobalt silicides have dopant diffusion and segregation coefficients that allow for formation of shallow conformal source and drain junctions, as illustrated in FIG. 4. After deposition of the metal layer 260, a heating cycle is performed. The heating cycle is used to react the portions of metal layer 260 which overlie the source extension 228 and the drain extension 230 as well as the source and drain regions 222. If the metal layer 260 comprises cobalt and the semiconductor layer 213 is silicon, then the cobalt reacts with the silicon within interface regions to form cobalt silicide ($CoSi_2$). Typical heat cycle temperatures for silicide/salicide formation range from 200 °C to 700 °C depending on the type of metal used. In all cases, silicided regions 264, shown in FIG. 5, (also referred to as salicided regions in self-aligned cases) are formed within the source and drain regions 222 via the heating cycle. All unreacted portions of the metal layer 260 are removed via known etch techniques without removing the silicided regions 264. For example, cobalt may be etched using an HCl and water isotropic etch chemistry.

Optionally, a liner oxide layer (not shown) may cover the exposed sidewalls of the gate electrode 36 and the dielectric layer 32. Such a thin liner oxide layer may be interposed between the top surface of the gate electrode 36 and the silicide layer 56. The liner oxide layer may be made of typical, well-known oxide materials, for example SiO_2. The liner oxide would act as a mask and prevent the metal layer from reacting with the polysilicon of the gate electrode 226. An exemplary liner oxide layer may have a thickness of about 10 Å.

It should be understood that at this time a metal layer 262 of the same or a different metal could be formed overlying the gate electrode 236 and processed as described above in a self-aligning process to produce a silicide layer 266 (shown in FIG. 5).

Next in step 718, a spacer 268 is formed using the process described above to protect the gate and a portion of the very thin silicide layers 264 which extend into the source and drain extensions 228, 230. Next, a metal layer 270 is deposited and heated as described above to form a multi-thickness silicide layer 272 of $CoSi_2$ (shown in FIG. 5) over the source and drain extension regions 228, 230, the main source and drain junction regions 250, 252 as well as the main source region 224 and the main drain region 226. The spacer 268 covering the portion of the silicide layer region 264 prevents the deposition of the metal layer 266 over the very thin portions of the silicide layers 264 overlying the source extension 228 and the drain extension 230 forming very thin silicide layer 254. The spacer 268 covering the gate and the thin silicide layers 254 is illustrated in FIG. 4.

It should be understood that a different metal could be formed overlying the silicide layer 264 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer 274 of the same or a different metal could be formed overlying the silicide layer 266 and processed as described above in a self-aligning process to produce a silicide layer 276 (shown in FIG. 6).

Thereafter, in step 720, a second spacer 278 is formed to protect a portion of the silicide layers 272 which overlie the junctions of the main source 250 and the main drain junction 252. Next, a metal layer 280 is deposited and heated as described above to form a multi-thickness silicide layer 282 (shown in FIG.1) of $CoSi_2$ over the source and drain regions 222. The spacers 268 and 278 covering the portions of the very thin silicide layers 254 and thin silicide layers 272 prevent the deposition of the metal layer 280 over the thin silicide layers 254, 272 overlying the source extension 228 and the drain extension 230 protected by the mask. The masks 268, 278 covering the gate and the thin silicide layers 264, 272 are illustrated in FIG. 6.

It should be understood that a different metal could be formed overlying the silicide layer 272 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer 282 of the same or a different metal could be formed overlying the silicide layer 276 and processed as described above in a self-aligning process to produce a silicide layer 56 (shown in FIG. 1). Thus, a device 210 having multi-thickness silicide may be produced.

Another embodiment of an SOI transistor device including multi-thickness silicide layers and successive spacers will now be described in accordance with the invention. The device includes a gate defining a channel interposed between a source and a drain and is disposed within one of the active regions of an SOI structure. Further, the device includes a multi-thickness silicide layer formed on the main source and drain

regions and the source and drain extension regions as will be described in more detail below. Further still, the device also includes a plurality of spacers used in the formation of the device wherein a first spacer is formed on the gate side wall. A second spacer is formed on the first spacer. Optionally, a third spacer or more may be formed on the preceding spacer. Additionally, a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the multi-thickness silicide layer which is formed on the main source and drain regions. The device may include a further silicide layer formed on a polysilicon electrode of the gate. Further still, the multi-thickness silicide layers may include at least two layers of silicide of two different species.

Referring initially to FIG. 8, an SOI transistor device of the present invention is shown generally designated as 10'. The SOI transistor device 10' is formed within a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 12, a buried oxide (BOX) layer 14 formed on the semiconductor substrate 12, and a semiconductor layer 13 disposed on the BOX layer 14. Within the semiconductor layer 13, shallow trench isolation (STI) regions 16 along with the BOX region 14 define the semiconductor active regions 18 of which one is shown in FIG. 8.

In an exemplary embodiment, as illustrated in FIG. 8, the active region 18 is a p-type region, or channel 20, and two N+ (source and drain) regions 22. The channel 20 is interposed between the source and drain regions 22. Alternatively, an n-type channel could be interposed between two P+ regions as will be readily appreciated. The source and drain regions 22 include respective deep implant regions 24 and 26, as well as respective extension regions 28 and 30. A gate dielectric 32 is interposed between a lower surface 34 of a gate electrode 36 and an upper surface 38 of the SOI semiconductor substrate 40. The gate dielectric 32 illustrated in FIG. 8 is a single layer dielectric, however the gate dielectric could be a multi-layer dielectric.

Multi-thickness silicide layers 42, 44 are disposed on a portion of the source and drain regions 22. Silicide regions 48 are formed on the polysilicon regions of the respective deep implant regions 24 and 26 and the respective deep implant junction regions 50 and 52. Very thin silicide regions 54 are formed over the respective extension regions 28 and 30. The multi-thickness silicide layers 42, 44 may be made of typical, well-known silicides, such as cobalt silicide ($CoSi_2$), titanium silicide ($TiSi_2$), tantalum silicide ($TaSi_2$), nickel silicide ($NiSi_2$) or the like. In an exemplary embodiment, the multi-thickness silicide layers 42, 44 are of $CoSi_2$. Silicide regions 48 could have a thickness of between 50 Å and 250 Å. Very thin silicide regions 54 could have a thickness of between 25 Å and 100 Å.

On top of the gate electrode 36 is a silicide layer 76. The silicide layer 76 may be made of the same suitable silicide materials described above. The silicide layer 76 may be made of the same material as the silicide layers 42, 44 or may be made of another silicide material described above. An exemplary silicide layer 76 may have a thickness of between 100 Å and 200 Å.

Spacer 68 extends upward from the upper surface 38 of the SOI substrate 40 encompassing the gate dielectric 32 and gate electrode 36. Spacer 78 extends upward from the upper surface 38 of the SOI substrate 40 encompassing spacer 68. The spacers 68 and 78 are permanent spacers used in the formation of the multi-thickness layers 42, 44, as well as the source and drain regions 22 which will further be described below.

It will be appreciated that the active region 18, the channel 20, the source and drain regions 22, the gate dielectric 32, the gate electrode 36, the silicide layer 76, the multi-thickness silicide layers 42, 44, and the successive spacers together form the SOI transistor device of the present invention. The principles of operation of an SOI transistor having multi-thickness silicide layers over the source and the drain regions of the gate device will be further explained below. It will be appreciated that the SOI transistor device 10' may alternatively have other shapes than the shape shown in FIG. 8.

The steps of a method 1510 for fabricating a semiconductor device 310 (which may be similar to the semiconductor device 10' described above) are outlined in the flow chart shown in FIG. 15. FIGS. 9 - 14 illustrate various steps of the method 1510. It will be appreciated that the method 1510 and the semiconductor device 310 described below are merely exemplary, and that suitable embodiments of the many above-described variations in materials, thicknesses, and/or structures may alternatively be used in the method 1510 and/or the semiconductor device 310.

In step 1512, a conventional polysilicon gate is formed on an SOI substrate as an intermediate stage of manufacture for the SOI transistor device 310. As shown in FIG. 9, the SOI transistor device 310 includes a semiconductor substrate 312, a BOX layer 314 formed on the semiconductor substrate 312 and a semiconductor layer 313 disposed on the BOX layer 314. An exemplary BOX layer may have a thickness of between 1800 Å and 2200 Å. Whereas, an exemplary semiconductor layer 313 disposed on the BOX layer 314 may have a thickness of between 800 Å and 1000 Å. Suitable semiconductor materials such as silicon, carbide, germanium or the like may be used as the semiconductor layer 313 disposed on the BOX layer 314. Within the semiconductor layer 313 disposed on the BOX layer 314, are shallow trench isolation (STI) regions 316 which along with the BOX layer 314 define the location of a semiconductor active region 318 for a future step. The STI regions 316 are insulator-filled to electrically isolate individual electrical devices such as the SOI transistor device 310. Other isolation techniques that are known in the art may be used to isolate the SOI transistor device 310.

A gate dielectric 332 is interposed between the lower surface 334 of a gate electrode 336 and an upper surface 338 of a portion of the SOI semiconductor substrate 340. The gate dielectric 332 illustrated in FIG. 9 is a single-layer dielectric, however the gate dielectric could be a multi-layer dielectric as described above. The gate dielectric 332 may be made of suitable gate dielectric materials, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), silicon oxynitride (SiNO) or the like. In this embodiment, dielectric layer 332 is made of Si_3N_4. The exemplary dielectric layer 332 of Si_3N_4 may have a thickness of between 13 Å and 16 Å. The gate electrode 336 may be made of typical, well-known conductive materials, for example polysilicon. An exemplary gate electrode 336 may have a thickness of between 800 Å and 1200 Å.

A more detailed description of an implantation process which will create the source and drain regions 322 which may be performed after the gate formation, is described below. In this exemplary embodiment, the channel region 320 underneath the gate dielectric 332, interposed between the source and the drain regions 322 is p-type doped prior to this step by either alternative described above.

In step 1514, the source and drain extension regions 328, 330 are formed as shown in FIG. 10. Prior to the source and drain extension formation, the semiconductor layer 313 of semiconductor substrate 340 may be appropriately doped to form a region or layer of electrically-active material for eventual use as an active region of the SOI transistor device 310 to be formed. For instance, boron or indium may be implanted to form a p-type region or channel for an n-type device and phosphorous or arsenic may be implanted to form an n-type region or channel for a p-type device. It should be understood that the semiconductor layer 313 could be appropriately doped prior to gate formation.

After formation of the gate, the lightly doped source and drain extension regions 328, 330 may be formed using techniques well known in the art for forming such extension layers. An extension perpendicular implant is a relatively low energy, low concentration implant which is capable of producing the source and drain extensions 328 and 330. The total concentration of the extension implants may be, for example, between $1X10^{18}$ atoms/cm^3 and $1X10^{18}$ atoms/cm^3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm^2. The extension perpendicular implants may be of the same material as the main perpendicular implant, or may alternatively include different materials. It should also be appreciated that the extension implants may be different from one another, if so desired.

Next in step 1516, a permanent spacer 368 may be formed around the gate to protect the gate electrode 336 and future extension regions 328, 330 from dopants used in the formation of the main source and the drain regions 326, 328 in a later step. In order to form the permanent space, a spacer material such as an oxide material, for example silicon dioxide (SiO_2), silicon nitride (Si_3N_4) or the like, is then deposited on the substrate 340 (not shown). The deposition produces an oxide layer upon a top surface 338 of the SOI substrate 340. The oxide deposition may be performed, for example, by plasma enhanced chemical vapor deposition (PECVD).

The oxide is etched with a suitable etchant. The substrate oxide layers are reduced in size, leaving oxide spacers similar to spacers 368 shown in FIG. 11. The oxide spacer may extend from a surface 338 of the semiconductor substrate 340 to a height of between 3000 Å and 4000 Å.

Thereafter, in step 1518, a metal layer 360 is formed overlying the source and drain extension layers 328, 330. The metal layer 360 is formed by one of either sputtering, chemical vapor deposition (CVD), or evaporation. The metal layer 360 may comprise any metal such as platinum, titanium, tantalum, nickel, cobalt, tungsten, and/or the like. In an exemplary embodiment, cobalt is used to form metal layer 360. Cobalt is preferred due to the fact that cobalt silicides have dopant diffusion and segregation coefficients that allow for formation of shallow conformal source and drain junctions, as illustrated in FIG. 12. After deposition of the metal layer 360, a heating cycle is performed. The heating cycle is used to react the portions of metal layer 360 which overlie the source extension 328 and the drain extension 330. If the metal layer 360 comprises cobalt and the semiconductor layer 313 is silicon, then the cobalt reacts with the silicon within interface regions to form cobalt silicide ($CoSi_2$). Typical heat cycle temperatures for silicide/salicide formation range from 200 °C to 700 °C depending on the type of metal used. In all cases, silicided regions 364, shown in FIG. 13, (also referred to as salicided regions in self-aligned cases) are formed within the source and drain regions 322 via the heating cycle. All unreacted portions of the metal layer 360 are removed via known etch techniques without removing the silicided regions 364. For example, cobalt may be etched using an HCl and water isotropic etch chemistry.

It should be understood that at this time a metal layer 362 of the same or a different metal could be formed overlying the gate electrode 336 and processed as described above in a self-aligning process to produce a silicide layer 366 (shown in FIG. 13).

Next in step 1520, a permanent spacer 378 may be formed around the spacer 368 to protect the very thin silicide layer 354 and future extension regions 328, 330 from dopants used in the formation of the main source and the drain regions 326, 328 in a later step. The spacer is formed using a technique described above or other techniques known in the art.

Now in step 1522, the main source and drain regions may be formed by a main perpendicular implant, which will not affect the extension implant regions due to the spacers 368, 378 acting as masks. The main perpendicular implant is a relatively high energy, high concentration implant which is capable of producing the source and drain deep implant regions 324 and 326. An exemplary range of concentration of these dopants is between $1X10^{18}$ and $1X10^{18}$ atoms/cm^3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm^2. The main perpendicular implants may be of the same material or may alternatively include different materials.

It will be appreciated that many alternative sequences or steps may be used to accomplish the implantation. Additionally, although the extension implantation and the main implantation are illustrated as each involving one implant, it will be appreciated that a greater number of implants may be employed. Further, halo implants may be used in forming the extension implantation after gate 336 patterning or/and spacer 368, 378 formation. For example, tilt angle extension implants (35-45 degrees) implanting In or BF_2 utilizing four rotations for a total implantation dose between $3.5X10^{13}$ and $5X10^{13}$ atoms/cm2 with energies 30-80 keV. Thus, the source and drain regions 322 are formed.

After implantation, the semiconductor device 310 may be subjected to rapid thermal annealing (RTA) at this time or at a later time. Exemplary RTA may be performed for between five and fifteen seconds at a temperature of 1,020 - 1,050°C.

A third spacer 380 is formed in step 224 in a manner described above. The spacer 380 is formed over the spacer 378 and any exposed portion of spacer 368. It should be understood that spacer 380 may be formed only over spacer 378 provided that spacer 378 completely covers 368.

Next in step 1526, a metal layer 382 is deposited and heated as described above to form a multi-thickness silicide layer 372 of $CoSi_2$ (shown in FIG. 14) over the main source and drain junction regions 350, 352 as well as the main source region 324 and the main drain region 326. The spacer 368 covering the portion of the silicide layer region 364 prevents the deposition of the metal layer 366 over the very thin portions of the silicide layers 364 overlying the source extension 328 and the drain extension 330 forming very thin silicide layer 354.

It should be understood that a different metal could be formed overlying the silicide layer 364 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer 384 of the same or a different metal could be formed overlying the silicide layer 366 and processed as described above in a self-aligning process to produce a silicide layer 76 (shown in FIG. 8).

Thereafter, in step 1528, a fourth or subsequent spacer may be formed to protect a portion of the silicide layers which overlies the main source and drain regions 322. Next, a metal layer may be deposited and heated as described above to form a multi-thickness silicide layer of $CoSi_2$ over the source and drain regions 322. The spacers covering the portions of the preceding silicide layers prevent the deposition of the metal layer over such layers. Thus, a multi-thickness silicide layer may be tailored to the application of the device.

It should be understood that a different metal could be formed overlying the silicide layer 360 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer 382 of the same or a different metal could be formed overlying the silicide layer 364 and processed as described above in a self-aligning process to produce a silicide layer 42, 44 (shown in FIG. 8). Thus, a device 10' having multi-thickness silicide may be produced.

An SOI transistor device including multi-thickness silicide layers will now be described in accordance with another embodiment of the present invention. The device includes a gate defining a channel interposed between a source and a drain and is disposed within one of the active regions of an SOI structure. Further, the device includes a multi-thickness silicide layer formed on the main source and drain regions and the source and drain extension regions as will be described in more detail below. Further still, the device also includes a single permanent spacer used in the formation of the device created from a disposable spacer formed on a side wall of the gate. Optionally, the disposable spacer may be formed in such a manner that it may be selectively etched multiple times during the process to tailor the multi-thickness silicide as required by the application of the device.

Additionally, a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the multi-thickness silicide layer which is formed on the main source and drain regions. The device may include a further silicide layer formed on a polysilicon electrode of the gate. Further still, the multi-thickness silicide layers may include at least two layers of silicide of two different species. Even further still, the multi-thickness silicide layers formed over the source and drain regions and silicide layer formed over the polysilicon electrode may be of different species. Further still a self aligned structure is formed without new masking needed.

Referring initially to FIG. 16, an SOI transistor device of the present invention is shown generally designated as 10". The SOI transistor device 10" is formed within a semiconductor-on-insulator (SOI) structure having a semiconductor substrate 12, a buried oxide (BOX) layer 14 formed on the semiconductor substrate 12, and a semiconductor layer 13 disposed on the BOX layer 14. Within the semiconductor layer 13, shallow trench isolation (STI) regions 16 along with the BOX region 14 define the semiconductor active regions 18 of which one is shown in FIG. 16.

In an exemplary embodiment, as illustrated in FIG. 16, the active region 18 is a p-type region, or channel 20, and two N+ (source and drain) regions 22. The channel 20 is interposed between the source and drain regions 22. Alternatively, an n-type channel could be interposed between two P+ regions as will be readily appreciated. The source and drain regions 22 include respective deep implant regions 24 and 26, as well as respective extension regions 28 and 30. A gate dielectric 32 is interposed between a lower surface 34 of a gate

electrode 36 and an upper surface 38 of the SOI semiconductor substrate 40. The gate dielectric 32 illustrated in FIG. 16 is a single layer dielectric, however the gate dielectric could be a multi-layer dielectric.

Multi-thickness silicide layers 42, 44 are disposed on a portion of the source and drain regions 22. Silicide regions 48 are formed on the polysilicon regions of the respective deep implant regions 24 and 26 and the respective deep implant junction regions 50 and 52. Very thin silicide regions 54 are formed over the respective extension regions 28 and 30. The multi-thickness silicide layers 42, 44 may be made of typical, well-known silicides, such as cobalt silicide ($CoSi_2$), titanium silicide ($TiSi_2$), tantalum silicide ($TaSi_2$), nickel silicide ($NiSi_2$) or the like. In an exemplary embodiment, the multi-thickness silicide layers 42, 44 are of $CoSi_2$. Silicide regions 48 could have a thickness of between 50 Å and 250 Å. Very thin silicide regions 54 could have a thickness of between 25 Å and 100 Å.

On top of the gate electrode 36 is a silicide layer 76. The silicide layer 76 may be made of the same suitable silicide materials described above. The silicide layer 76 may be made of the same material as the silicide layers 42, 44 or may be made of another silicide material described above. An exemplary silicide layer 76 may have a thickness of between 100 Å and 200 Å.

Spacer 68 extends upward from the upper surface 38 of the SOI substrate 40 forming on the side walls of the gate dielectric 32 and the gate electrode 36. The spacer 68 is a permanent spacer used in the formation of the very thin silicide regions 54 which will further be described below.

It will be appreciated that the active region 18, the channel 20, the source and drain regions 22, the gate dielectric 32, the gate electrode 36, the silicide layer 76, the multi-thickness silicide layers 42, 44, and the permanent spacer together form the SOI transistor device of the present invention. The principles of operation of an SOI transistor having multi-thickness silicide layers over the source and the drain regions of the gate device will be further explained below. It will be appreciated that the SOI transistor device 10" may alternatively have other shapes than the shape shown in FIG. 16.

The steps of a method 2310 for fabricating a semiconductor device 410 (which may be similar to the semiconductor device 10" described above) are outlined in the flow chart shown in FIG. 23. FIGS. 17 - 22 illustrate various steps of the method 2310. It will be appreciated that the method 2310 and the semiconductor device 410 described below are merely exemplary, and that suitable embodiments of the many above-described variations in materials, thicknesses, and/or structures may alternatively be used in the method 2310 and/or the semiconductor device 410.

In step 2312, a conventional polysilicon gate is formed on an SOI substrate as an intermediate stage of manufacture for the SOI transistor device 410. As shown in FIG. 17, the SOI transistor device 410 includes a semiconductor substrate 412, a BOX layer 414 formed on the semiconductor substrate 412 and a semiconductor layer 413 disposed on the BOX layer 414. An exemplary BOX layer 414 may have a thickness of between 1800 Å and 2200 Å. Whereas, an exemplary semiconductor layer 413 disposed on the BOX layer 414 may have a thickness of between 800 Å and 1000 Å. Suitable semiconductor materials such as silicon, carbide, germanium or the like may be used as the semiconductor layer 413 disposed on the BOX layer 414. Within the semiconductor layer 413 disposed on the BOX layer 414, are shallow trench isolation (STI) regions 416 which along with the BOX layer 414 define the location of a semiconductor active region 418 for future processing.

The STI regions 416 are insulator-filled to electrically isolate individual electrical devices such as the SOI transistor device 410. Other isolation techniques that are known in the art may be used to isolate the SOI transistor device 410.

A gate dielectric 432 is interposed between the lower surface 434 of a gate electrode 436 and an upper surface 438 of a portion of the SOI semiconductor substrate 440. The gate dielectric 432 illustrated in FIG. 17 is a single-layer dielectric, however the gate dielectric could be a multi-layer dielectric as described above. The gate dielectric 432 may be made of suitable gate dielectric materials, such as silicon dioxide (SiO_2), silicon nitride (Si_3N_4), aluminum oxide (Al_2O_3), hafnium oxide (HfO_2), silicon oxynitride (SiNO) or the like. In this embodiment, dielectric layer 432 is made of Si_3N_4. The exemplary dielectric layer 432 of Si_3N_4 may have a thickness of between 13 Å and 16 Å. The gate electrode 436 may be made of typical, well-known conductive materials, for example polysilicon. An exemplary gate electrode 436 may have a thickness of between 800 Å and 1200 Å.

A more detailed description of an implantation process which will create the source and drain regions 422 which may be performed after the gate formation, is described below. In this exemplary embodiment, the channel region 420 underneath the gate dielectric 432, interposed between the source and the drain regions 422 is p-type doped prior to this step by either alternative described below.

Prior to the gate formation, the semiconductor layer 413 of semiconductor substrate 440 may be appropriately doped to form a region or layer of electrically-active material for eventual use as an active region of the SOI transistor device 410 to be formed. For instance, boron or indium may be implanted to form a p-type region or channel for an n-type device and phosphorous or arsenic may be implanted to form an n-type region or channel for a p-type device. It should be understood that the semiconductor layer 413 could be appropriately doped after gate formation by techniques known in the art.

Next in step 2314, a disposable spacer 478 may be formed around the gate to protect the gate electrode 436 and future extension regions 428, 430 from dopants used in the formation of the main source and the drain regions 426, 428 in a later step. In order to form the disposable space, a spacer material such as an oxide material, for example silicon dioxide (SiO_2), silicon nitride (Si_3N_4) or the like, is then deposited on the substrate 440 (not shown). The deposition produces an oxide layer upon a top surface 438 of the SOI substrate 440. The oxide deposition may be performed, for example, by plasma enhanced chemical vapor deposition (PECVD). The disposable spacer 478 may be formed in such a manner as to be selectively etched in stages in order to tailor the formation of the multi-thickness silicide layers.

The oxide is etched with a suitable etchant. The substrate oxide layers are reduced in size, leaving oxide spacer similar to spacers 478 shown in FIG. 19. The oxide spacer may extend from a surface 438 of the semiconductor substrate 440 to a height of between 3000 Å and 4000 Å and a thickness between 500Å and 1000Å. The resultant structure is shown in FIG. 18.

Now in step 2316, the main source and drain regions may be formed by a main perpendicular implant, which will not affect the extension implant regions due to the spacer 478 acting as a mask. The main perpendicular implant is a relatively high energy, high concentration implant which is capable of producing the source and drain deep implant regions 424 and 426. An exemplary range of concentration of these dopants is

between $1X10^{18}$ and $1X10^{18}$ atoms/cm^3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm^2. The main perpendicular implants may be of the same material or may alternatively include different materials. The resultant structure is shown in FIG. 19.

Thereafter, in step 2318, a metal layer 460 is formed overlying the main source and drain regions 424, 426. The metal layer 460 is formed by one of either sputtering, chemical vapor deposition (CVD), or evaporation. The metal layer 460 may comprise any metal such as platinum, titanium, tantalum, nickel, cobalt, tungsten, and/or the like. In an exemplary embodiment, cobalt is used to form metal layer 460. Cobalt is preferred due to the fact that cobalt silicides have dopant diffusion and segregation coefficients that allow for formation of shallow conformal source and drain junctions, as illustrated in FIG. 22. After deposition of the metal layer 460, a heating cycle is performed. The heating cycle is used to react the portions of metal layer 460 which overlie the source and drain regions 424, 426. If the metal layer 460 comprises cobalt and the semiconductor layer 413 is silicon, then the cobalt reacts with the silicon within interface regions to form cobalt silicide ($CoSi_2$). Typical heat cycle temperatures for silicide/salicide formation range from 200 °C to 700 °C depending on the type of metal used. In all cases, silicided regions 464, shown in FIG. 21, (also referred to as salicided regions in self-aligned cases) are formed within the source and drain regions 422 via the heating cycle. All unreacted portions of the metal layer 460 are removed via known etch techniques without removing the silicided regions 464. For example, cobalt may be etched using an HCl and water isotropic etch chemistry.

It should be understood that at this time a metal layer 462 of the same or a different metal could be formed overlying the gate electrode 436 and processed as described above in a self-aligning process to produce a silicide layer 466 (shown in FIG. 21).

Next in step 2320, a portion of the disposable spacer 478 may be removed using an etchant known in the art. The result is the formation of permanent spacer 468 to protect gate electrode 436. Spacer 468 will also be used in the formation of the very thin silicide layer 454 over the extension regions 428, 430 to be formed in a process described below.

Now in step 2322, the source and drain extension regions 428, 430 are formed. After removal of the disposable spacer 478, the lightly doped source and drain extension regions 428, 430 may be formed using techniques well known in the art for forming such extension layers. An extension perpendicular implant is a relatively low energy, low concentration implant which is capable of producing the source and drain extensions 428 and 430. The total concentration of the extension implants may be, for example, between $1X10^{18}$ atoms/cm3 and $1X10^{18}$ atoms/cm3. An exemplary range of implant dose for the perpendicular implant is between $1X10^{15}$ and $2X10^{15}$ atoms/cm2. The extension perpendicular implants may be of the same material as the main perpendicular implant, or may alternatively include different materials. It should also be appreciated that the extension implants may be different from one another, if so desired. The resultant structure is shown in FIG. 21.

It will be appreciated that many alternative sequences or steps may be used to accomplish the implantation. Additionally, although the extension implantation and the main implantation are illustrated as each involving one implant, it will be appreciated that a greater number of implants may be employed. Further, halo implants may be used in forming the extension implantation after gate 436 patterning or/and spacer 468,

478 formation. For example, tilt angle extension implants (35-45 degrees) implanting In or BF_2 utilizing four rotations for a total implantation dose between $3.5X10^{13}$ and $5X10^{13}$ atoms/cm2 with energies 30-80 keV. Thus, the source and drain regions 422 are formed.

After implantation, the semiconductor device 410 may be subjected to rapid thermal annealing (RTA) at this time or at a later time. Exemplary RTA may be performed for between five and fifteen seconds at a temperature of 1,020 - 1,050°C.

Next in step 2324, a metal layer 453 is deposited and heated as described above to form a multi-thickness silicide layer 454 of $CoSi_2$ (shown in FIG. 16) over the source and drain extension regions 428, 430. The spacer 468 covering the portion of the silicon layer 413 controls the deposition of the metal layer 453 overlying the source extension 428 and the drain extension 430 and thereby controls how close the very thin silicide layer 454 comes to the source and drain extension junctions 486, 488.

It should be understood that a different metal could be formed overlying the silicide layer 466 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer 484 of the same or a different metal could be formed overlying the silicide layer 466 and processed as described above in a self-aligning process to produce a silicide layer 76 (shown in FIG. 16).

It should be understood that a different metal could be formed overlying the silicide layer 464 and processed as described above resulting in a silicide layer having both multi-thickness regions and multi-layers (not shown). Additionally, it should be understood that at this time a metal layer (not shown) of the same or a different metal could be formed overlying the silicide layer 464 and processed as described above in a self-aligning process to produce a silicide layer 42, 44 (shown in FIG. 16). Thus, a device 10" having multi-thickness silicide may be produced.

In alternative exemplary embodiments to the inventions described in the figures above, the source and drain regions 222, 322 or 422 can be formed using the process described below. An ion implant as described above may be used to dope the silicide regions 242, 244, 342, 344 or 442, 444 with dopant atoms. Either boron, arsenic, or phosphorus may be used alone or in any combination as the dopant atoms. Therefore, either an n-type channel transistor or a p-type channel transistor may be formed. In one embodiment, the dopant atoms are ion implanted at an energy which places the dopant atoms only in the silicided regions 242, 244, 342, 344 or 442, 444. Another heating cycle is used to drive the dopant atoms from the silicided regions 242, 244, 342, 344 or 442, 444 into the substrate 213, 313 or 413 to form the source and drain region 222, 322 or 422. In another embodiment, the ion implant of the dopant atoms may be performed at a high energy to ensure that the dopant atoms penetrate the silicided regions 242, 244, 342, 344 or 442, 444 and form the source and the drain region 222, 322 or 422. It is important to note that the ion implantation of the silicided regions 244, 344 or 444 to form the source and the drain region 222, 322 or 422 may be performed at any point in time in the process of FIGS. 2 - 6, 9 - 14 or 17 - 22. A self-aligned process is preferred but is optional.

After implantation, the semiconductor device 210, 310 or 410 is subjected to rapid thermal annealing (RTA). Exemplary RTA may be performed for between five and fifteen seconds at a temperature of 1,020-1,050°C.

In yet another exemplary embodiment, the semiconductor layer 213 is lightly doped and a polysilicon gate and the intermediate structure as illustrated in FIG. 1 is formed. The structure is lightly doped to form a thin lightly doped layer over the source and drain regions 222. A metal layer such as colbalt is deposited on the thin lightly doped layer and annealed as described above to form a thin silicide layer within the thin lightly doped region. It should be understood, that the same metal or a different metal layer may also be deposited on the polysilicon gate 236 to form a salicide structure. Next, a spacer may be formed using a process described above to protect a portion of the thin silicide layer. Now, a heavier doping may be done using a process described above in order to form the main source and drain regions 224, 226. Next, another metal layer, either the same or different than the previously deposited, is deposited and annealed as described above to form a thin silicide region overlying the main source and drain regions 224, 226. Thus, a device 210 having multi-thickness silicide may be produced. It should be understood that the process of forming spacers and depositing metal layers in order to form multi-thickness regions can be done numerous times in order to tailor the multi-thickness structure for the application it is being used for.

INDUSTRIAL APPLICABILITY

The electrical devices described above can tailor the resistance in the various regions such as the polysilicon regions of the source and drain regions, the junction regions of the source and drain regions, and the source and the drain extension regions. Further, in electrical devices on SOI structures the disadvantages due to the FBE can also be reduced.

Although the devices 10, 10' and 10" are illustrated as a transistor on an SOI structure, other devices such as electrically erasable programmable read only memories (EEPROMs), electrically programmable read only memories (EPROMs), flash EPROMs, thyristers, diodes, thin film transistors (TFTs), and the like may be formed on SOI structures as described above or on other types of substrates such as germanium-on-insulator (GOI). Further, such devices could also be formed on bulk substrates and benefit from the features of the above described invention.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto.

CLAIMS

What is claimed is:

1. A transistor device (10) formed on a semiconductor substrate (12) having active regions (18) defined by isolation trenches (16), the device comprising:

a gate (36) defining a channel (20) interposed between a source and a drain (22) formed within the active region of the semiconductor substrate wherein the source and the drain include main source and drain regions (24 and 26) and source and drain extension regions (28 and 30); and

a multi-thickness silicide layer (42 and 44) formed on the main source and drain regions and source and drain extension regions wherein a portion (54) of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion (46) of the silicide layer which is formed on the main source and drain regions.

2. The transistor device according to claim 1, including a plurality of spacers used in the formation of the device.

3. The transistor device according to claim 1, including a disposable spacer used in the formation of the device.

4. The transistor device according to any one of claims 1 to 3, wherein the semiconductor substrate is a semiconductor-on-insulator (SOI) substrate with a buried oxide (BOX) layer interposed between the active layer and a main semiconductor substrate and wherein the active regions are further defined by the BOX layer.

5. The transistor device according to claim 4, wherein the semiconductor-on-insulator substrate is a germanium-on-insulator (GOI) substrate.

6. The transistor device according to any one of claims 1 to 5, wherein the multi-thickness silicide layer includes at least two layers of silicide of different species.

7. The transistor device according to claim 6, wherein the least two layers of silicide of different species include;

a first silicide layer which is formed on the source and drain regions and extends into the extension regions;

a second silicide layer which is formed on the main source and drain regions.

8. The transistor device according to claim 6, wherein the least two layers of silicide of different species include;

a first silicide layer which is formed on the source and drain regions and extends into the extension regions with a thickness in a range between 25 Å and 100 Å; and

a second silicide layer which is formed on the main source and drain regions with a thickness in a range between 50 Å and 250 Å.

9. The transistor device according to any one of claims 1 to 5, including a second silicide layer formed on a polysilicon electrode of the gate.

10. The transistor device according to any one of claims 1 to 5, wherein the multi-thickness silicide layer which is formed on polysilicon regions of the main source and drain regions is thicker than the portion of the silicide layer which is formed on main junction regions of main source and drain regions.

11. The transistor device according to any one of claims 1 to 5, wherein the thickness of the portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is in a range between 25 Å and 100 Å.

12. The transistor device according to any one of claims 1 to 5, wherein the thickness of the portion of the multi-thickness silicide layer which is formed on the main source and drain regions is in a range between 50 Å and 250 Å.

13. The transistor device according to any one of claims 7 or 10, wherein the thickness of the portion of the multi-thickness silicide layer which is formed on polysilicon regions of the main source and drain regions is in a range between 100 Å and 300 Å.

14. The transistor device according to claim 2, wherein the plurality of spacers is permanent spacers formed in successive steps during a formation process of the device.

15. The transistor device according to claim 2, wherein a first spacer is formed on the gate side wall; and

a second spacer is formed on the first spacer.

16. The transistor device according to claim 2, wherein a third spacer is formed on the preceding spacer.

17. The transistor device according to claim 3, wherein a permanent spacer is formed from the disposable spacer.

18. The transistor device according to claim 3, wherein a first intermediate spacer is formed from the disposable spacer to control the formation of the source and drain the multi-thickness silicide layer.

19. The transistor device according to claim 3, wherein a second intermediate spacer is formed from the first intermediate spacer.

20. A method of fabricating a transistor device formed on a semiconductor substrate having active regions defined by isolation trenches, the method comprising the steps of:

forming a gate defining a channel interposed between a source and a drain formed within one of the active regions of the semiconductor substrate;

forming a multi-thickness silicide layer on the main source and drain regions and source and drain extension regions wherein a portion of the multi-thickness silicide layer which is formed on the source and drain extension regions is thinner than a portion of the silicide layer which is formed on the main source and drain regions.

21. The method according to claim 20, including the additional steps of:

forming a first spacer on a gate side wall;

forming a second spacer on the first spacer.

22. The method according to claim 20, including the additional steps of:

forming a disposable spacer on a side wall of the gate.

23. The method according to any one of claims 20 to 22, including the additional step of forming portions of the multi-thickness silicide layer on polysilicon regions of the main source and drain regions which are thicker than the portion of the multi-thickness silicide layer which is formed on the main junction regions of main source and drain regions.

24. The method according to any one of claims 20 to 22, wherein the semiconductor substrate is a semiconductor-on-insulator (SOI) substrate with a buried oxide (BOX) layer interposed between the active layer and a main semiconductor substrate and wherein the active regions are further defined by the BOX layer.

25. The method according to claim 24, including the additional step of forming portions of the multi-thickness silicide layer on polysilicon regions of the main source and drain regions which are thicker than the portion of the multi-thickness silicide layer which is formed on the main junction regions of main source and drain regions.

26. The method according to claim 21, including the additional step of forming a third spacer on the second spacer.

27. The method according to claim 27. Including the additional step of etching selectively the disposable spacer in stages in order to tailor the formation of the multi-thickness silicide layers.

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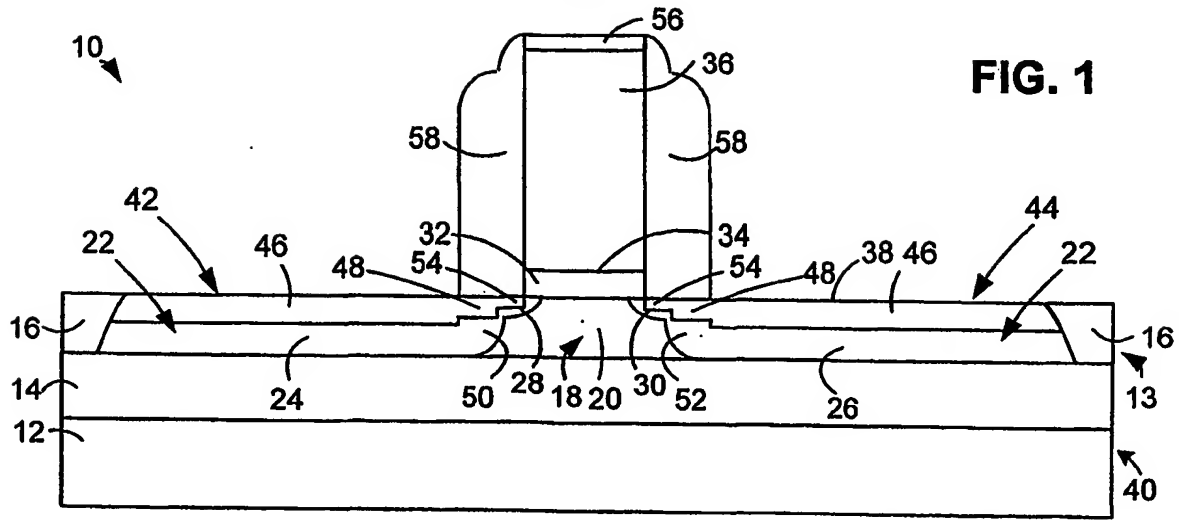


FIG. 1

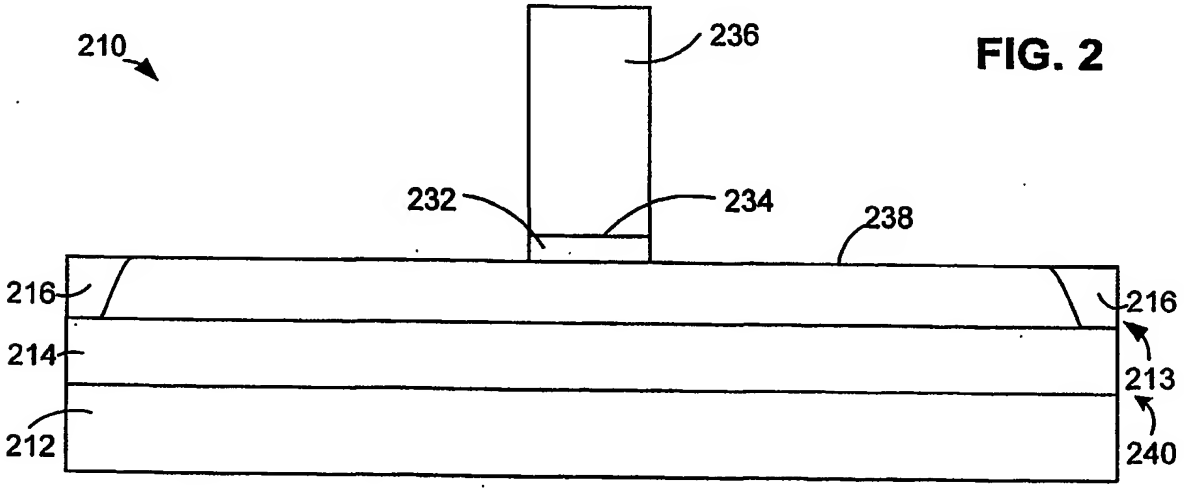


FIG. 2

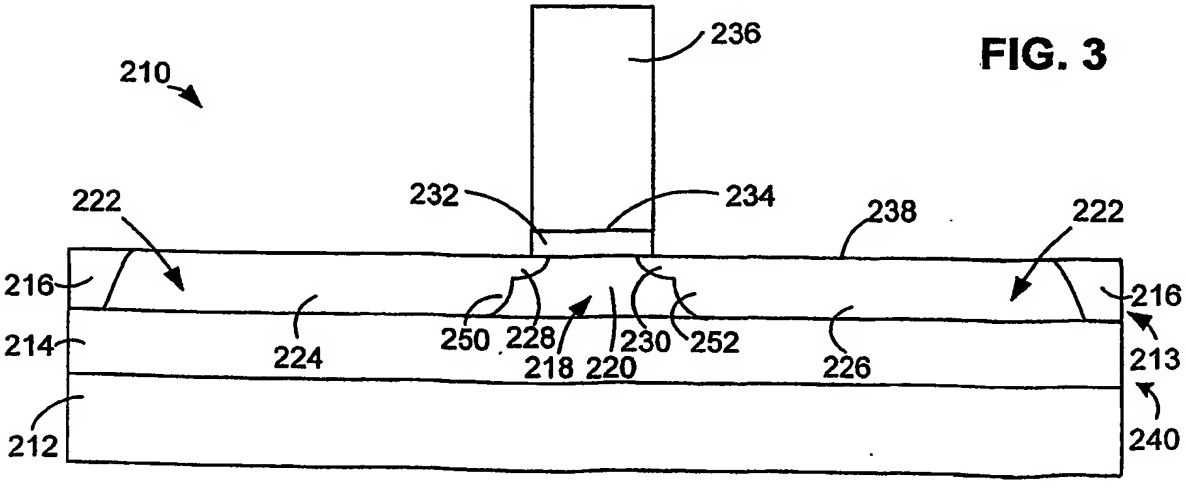


FIG. 3

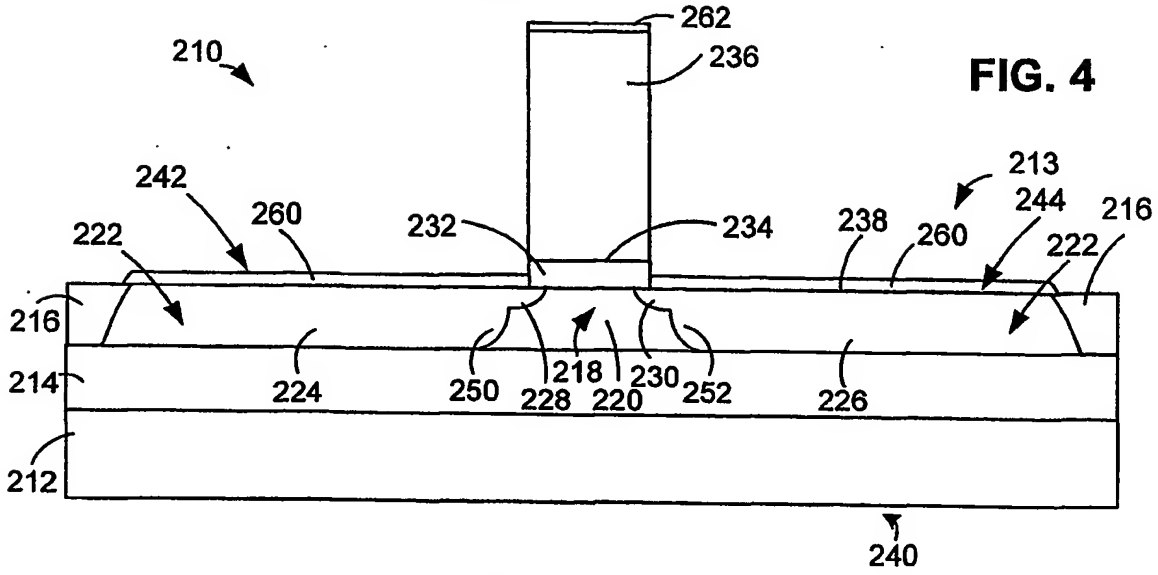


FIG. 4

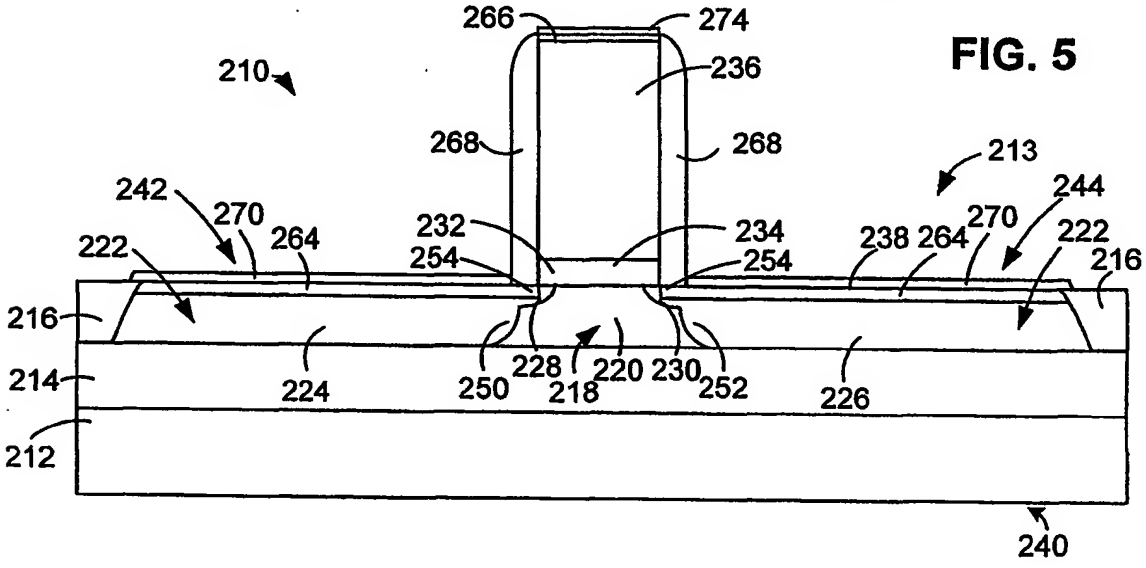


FIG. 5

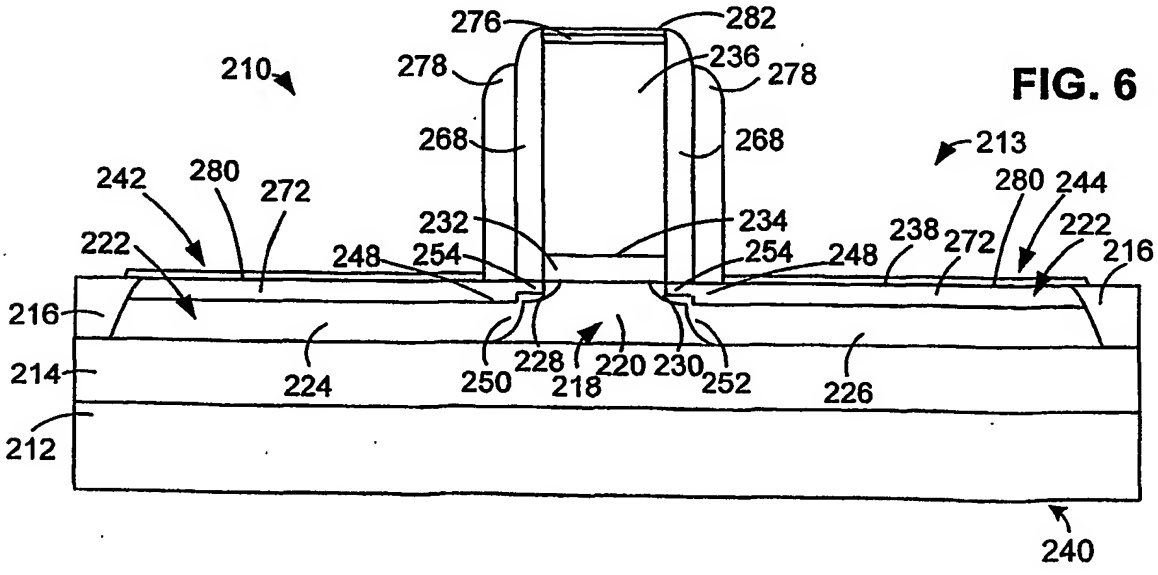


FIG. 6

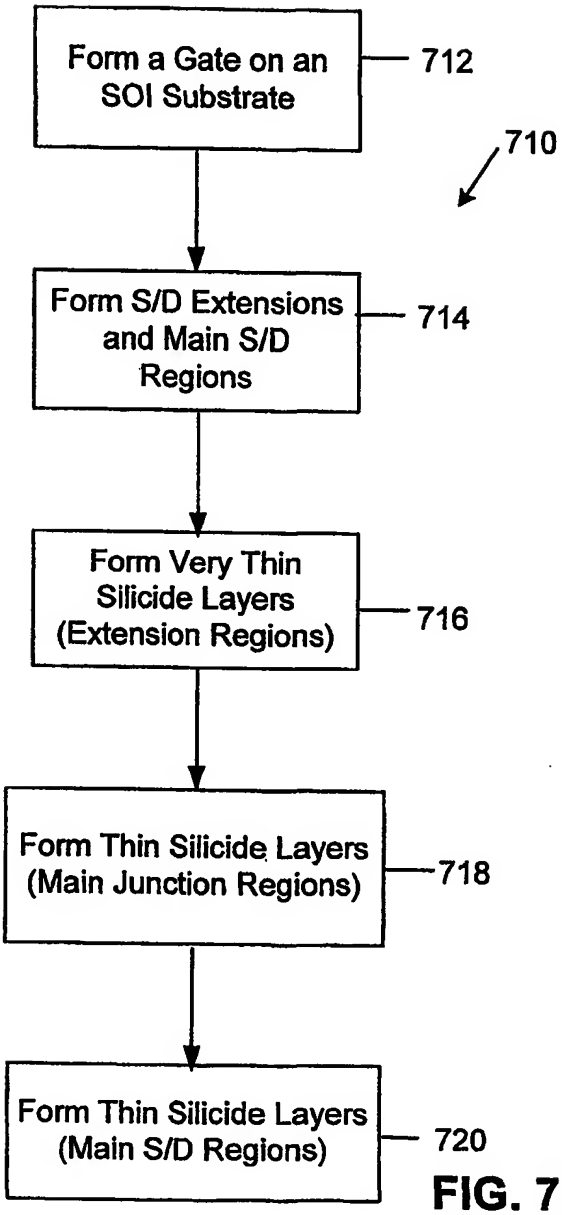

Form a Gate on an SOI Substrate
712
710
Form S/D Extensions and Main S/D Regions
714
Form Very Thin Silicide Layers (Extension Regions)
716
Form Thin Silicide Layers (Main Junction Regions)
718
Form Thin Silicide Layers (Main S/D Regions)
720

FIG. 7

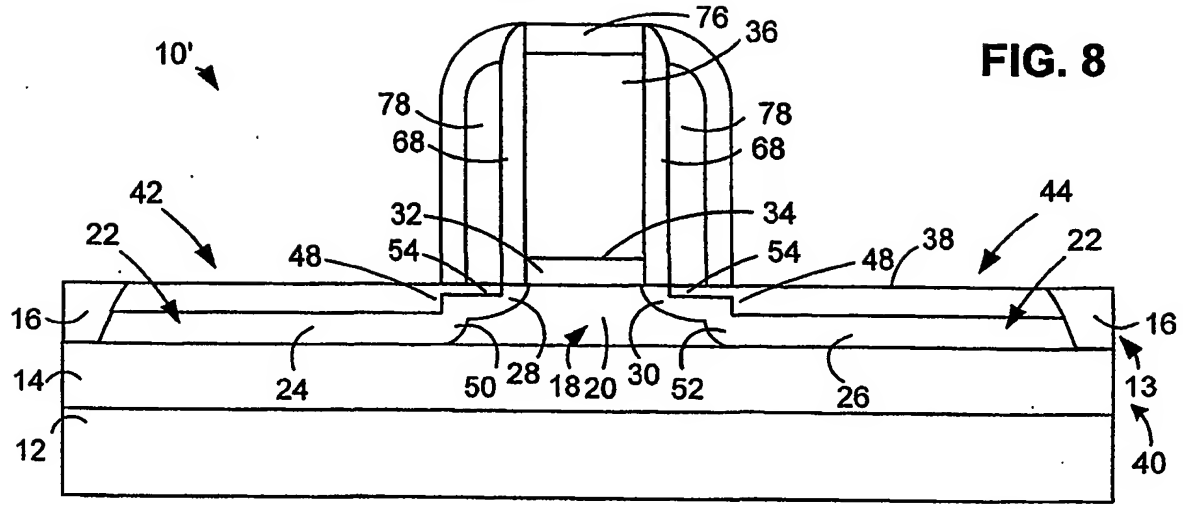


FIG. 8

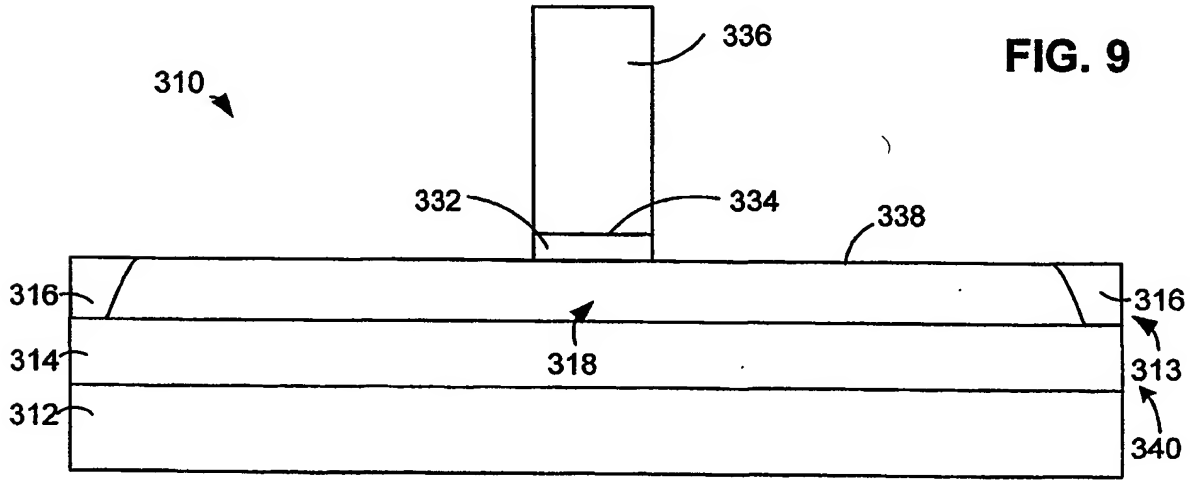


FIG. 9

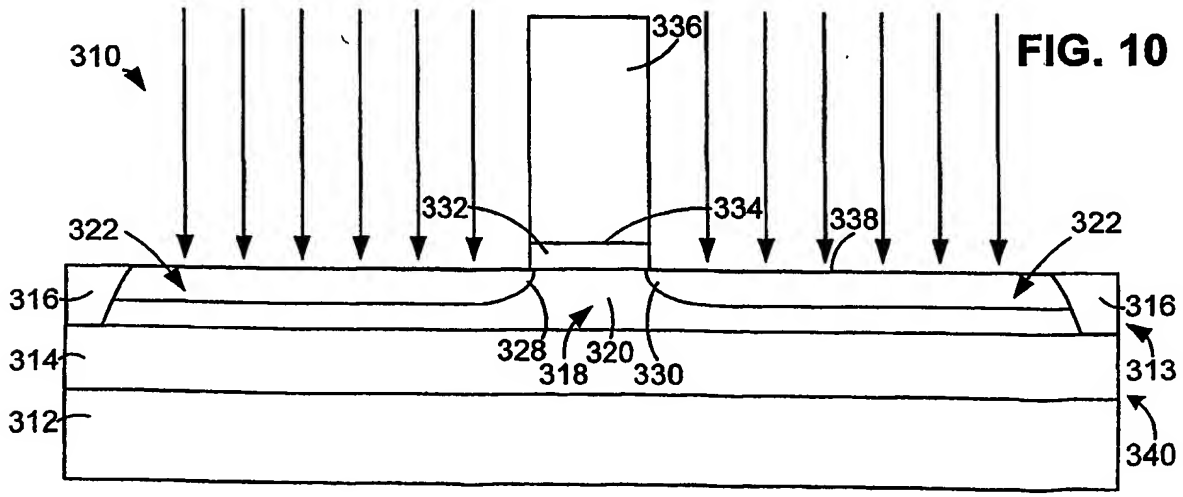


FIG. 10

FIG. 11

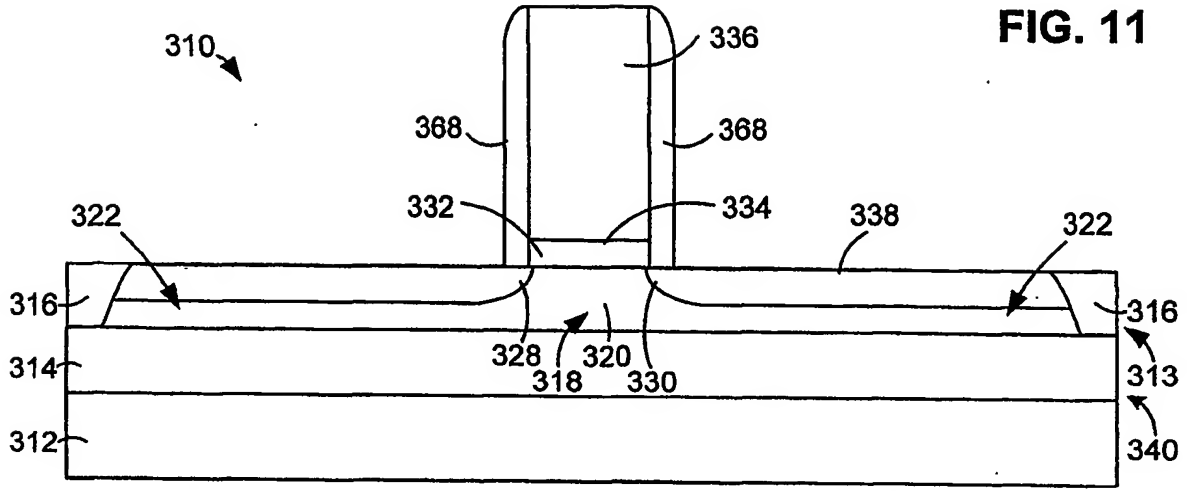


FIG. 12

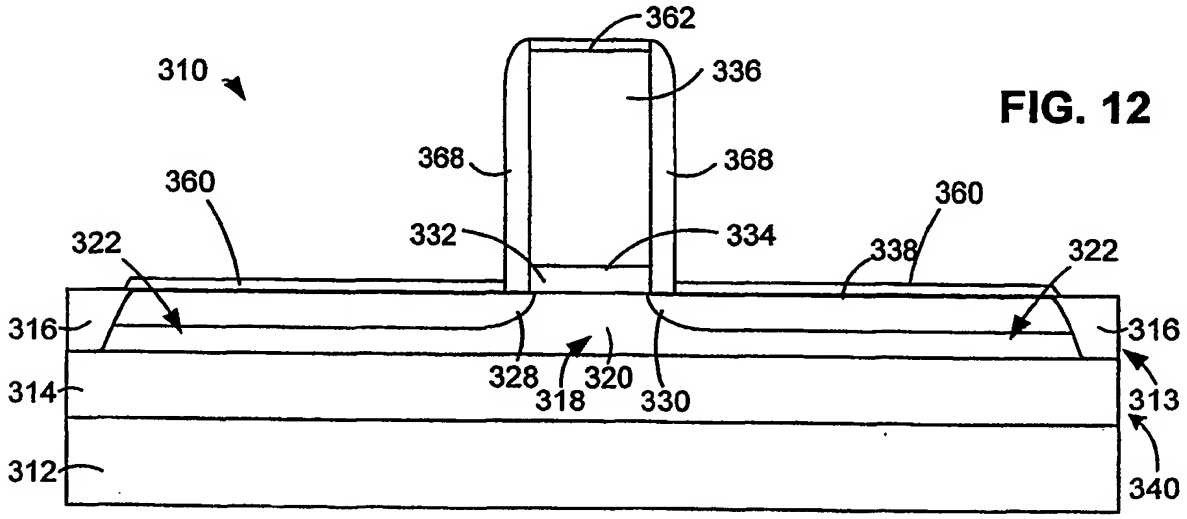
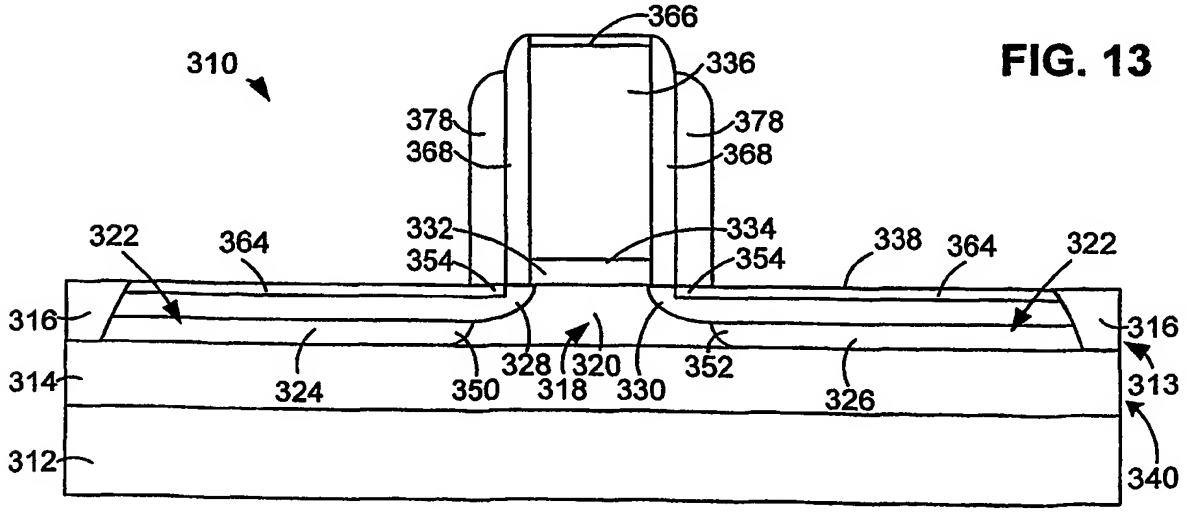


FIG. 13



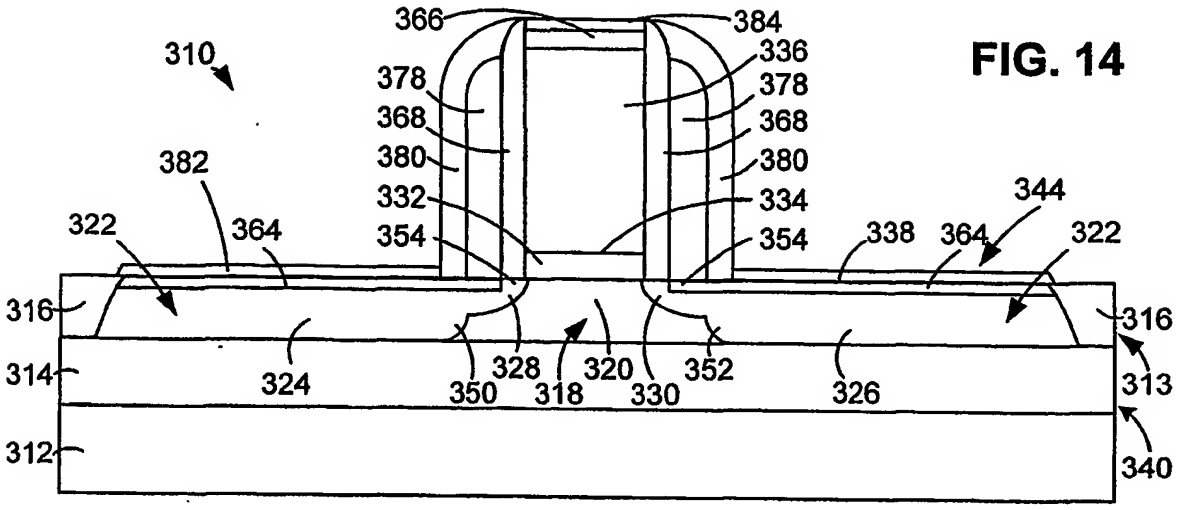

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FIG. 14

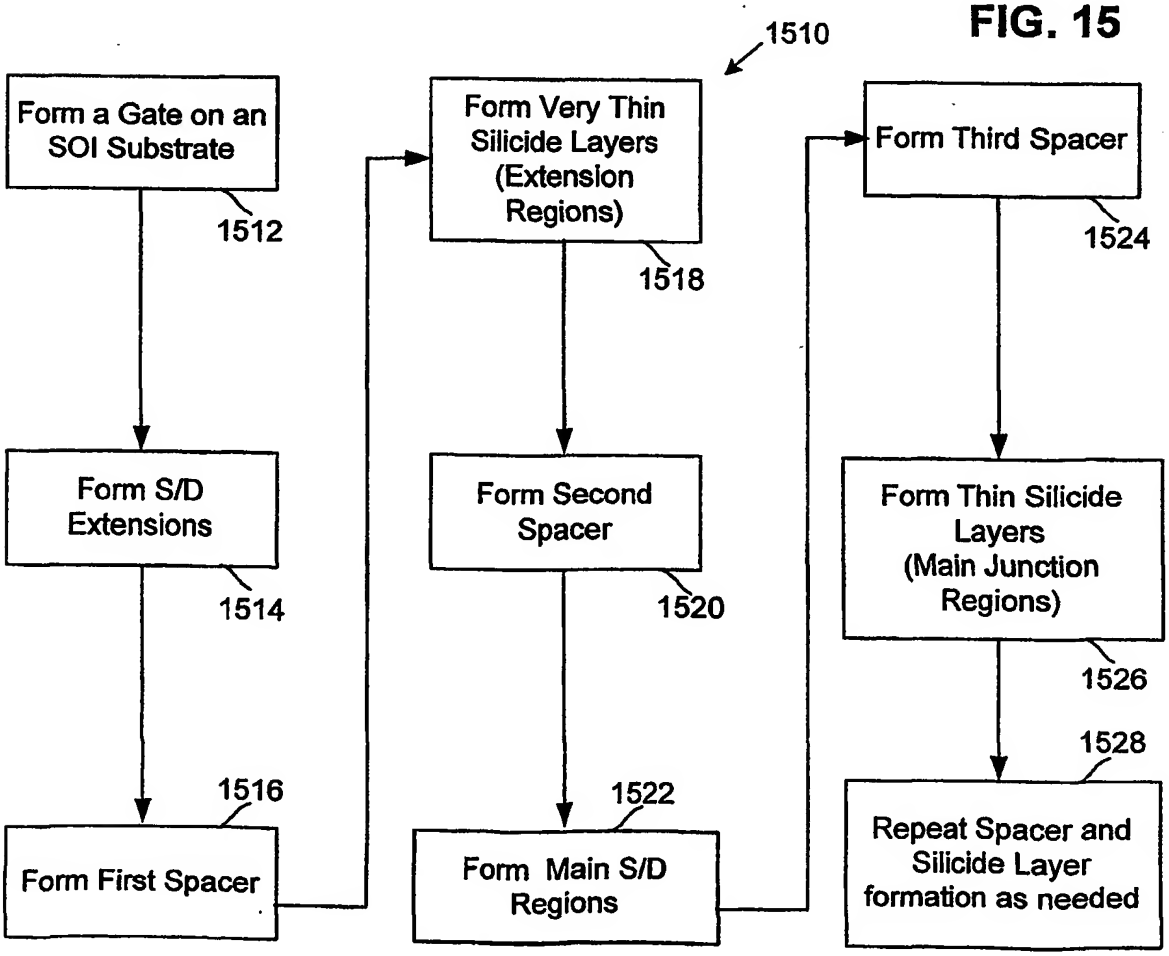
1510
Form a Gate on an SOI Substrate
1512
Form S/D Extensions
1514
Form First Spacer
1516
Form Very Thin Silicide Layers (Extension Regions)
1518
Form Second Spacer
1520
Form Main S/D Regions
1522
Form Third Spacer
1524
Form Thin Silicide Layers (Main Junction Regions)
1526
Repeat Spacer and Silicide Layer formation as needed
1528

FIG. 15

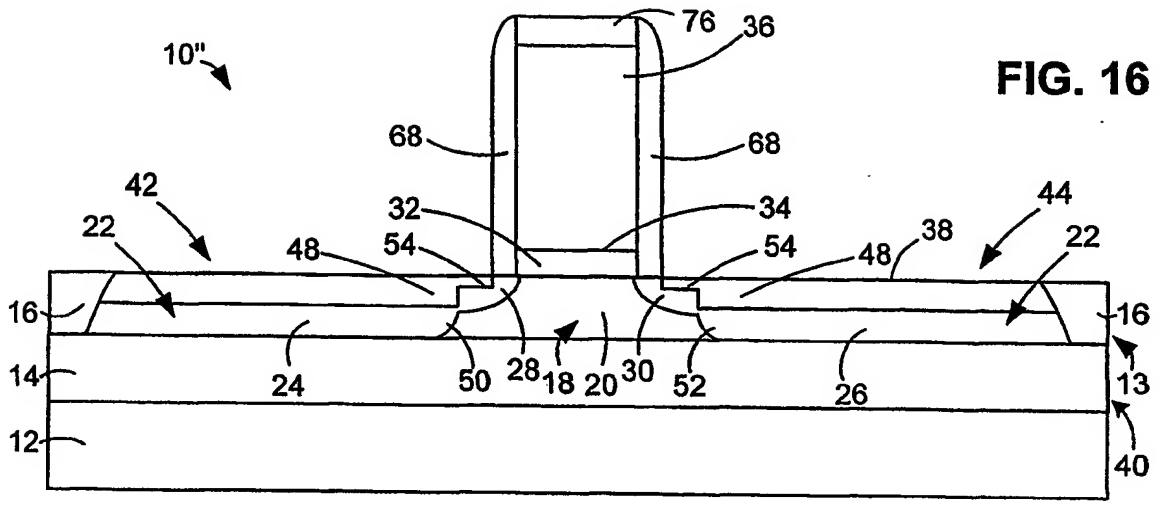

FIG. 16

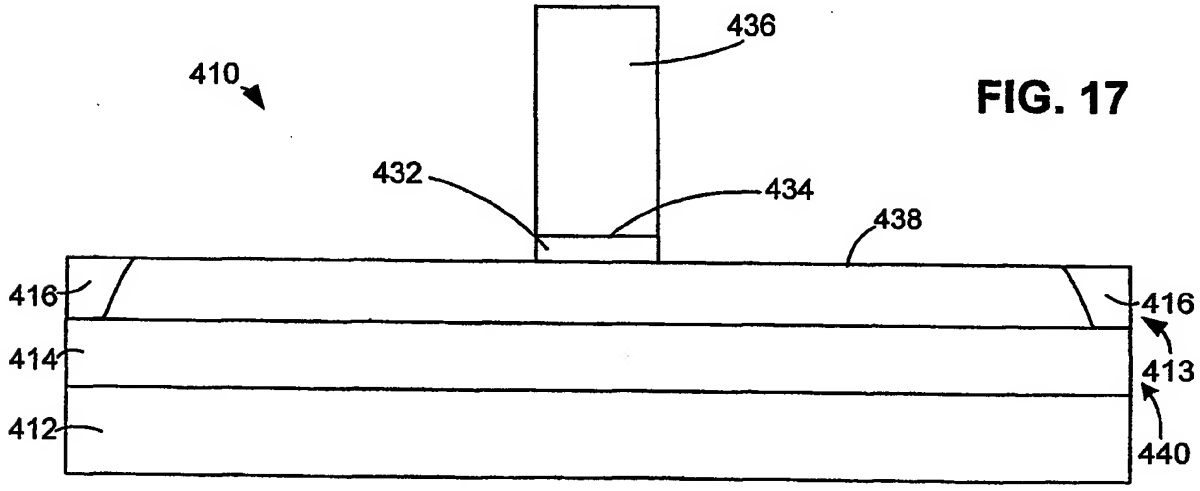

FIG. 17

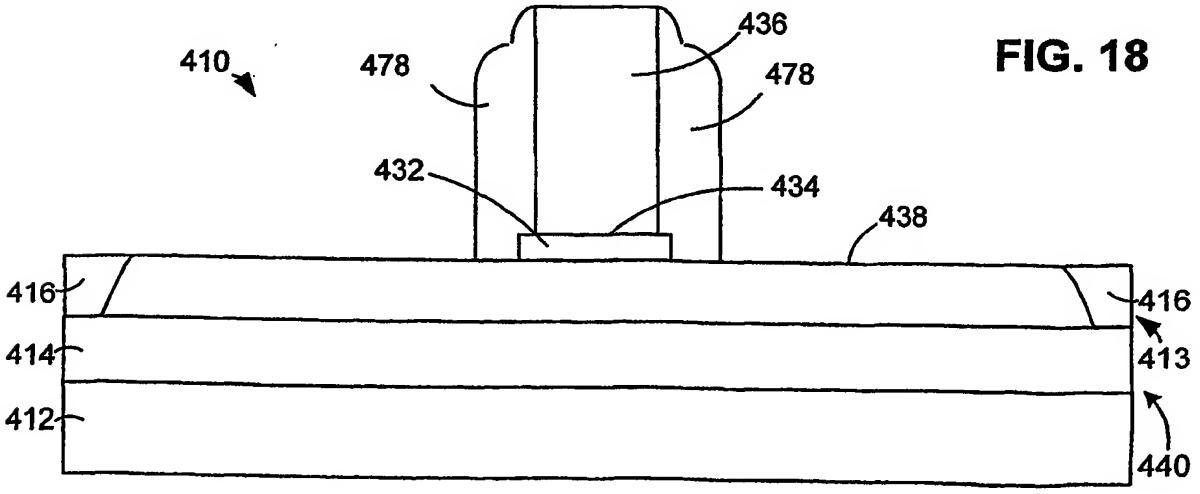

FIG. 18

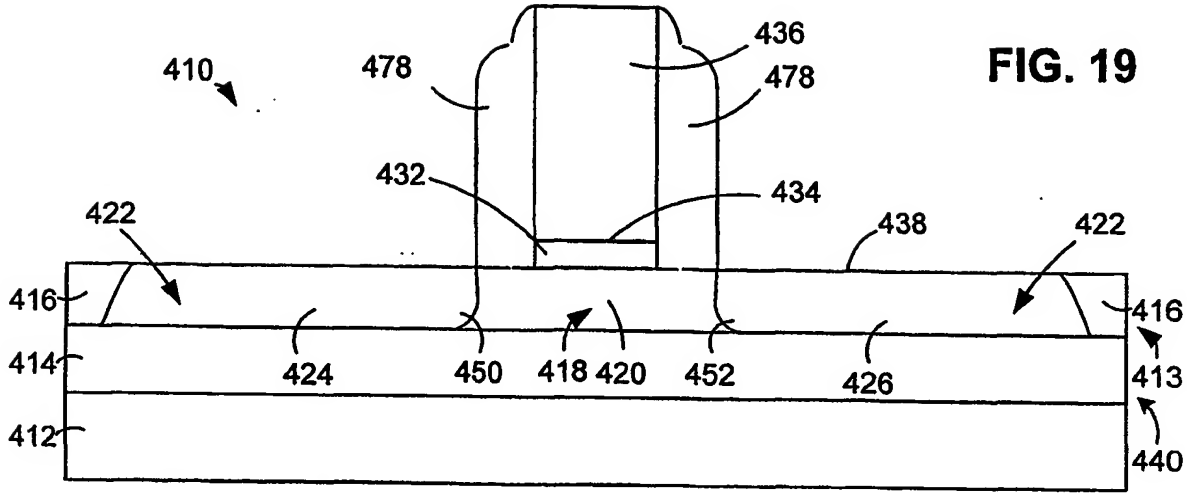

FIG. 19

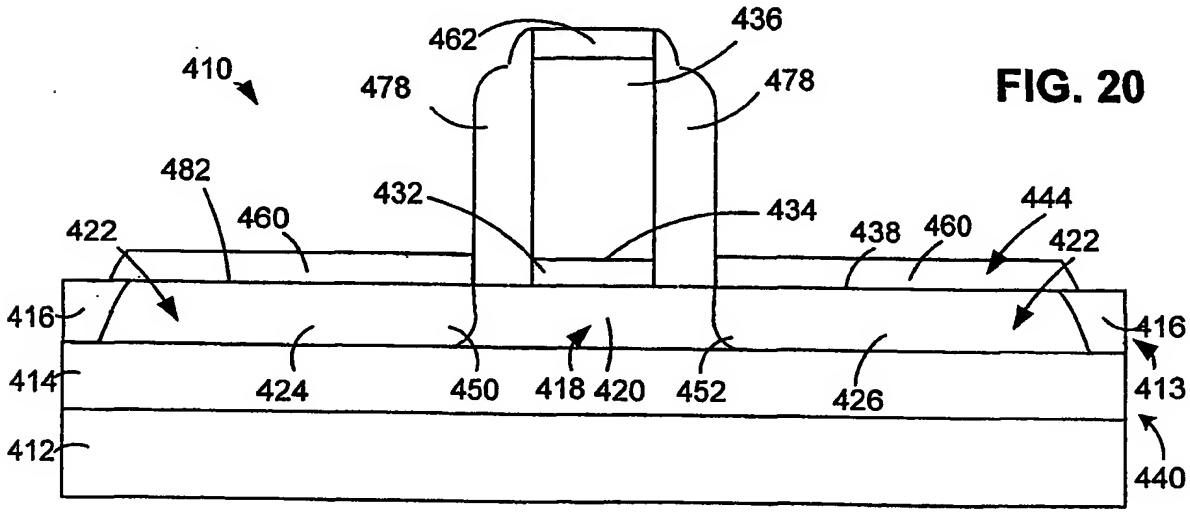

FIG. 20

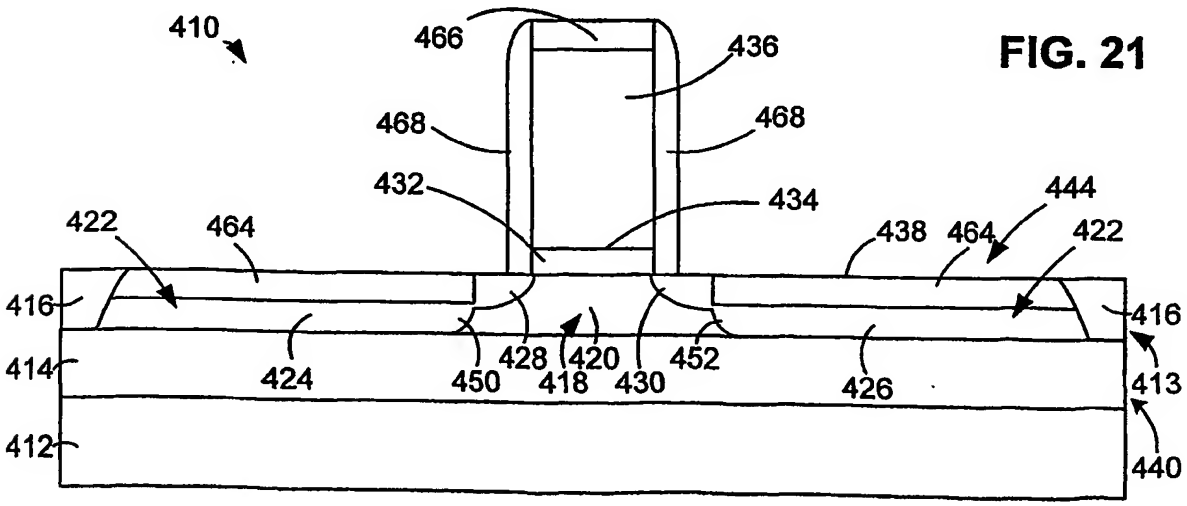

FIG. 21

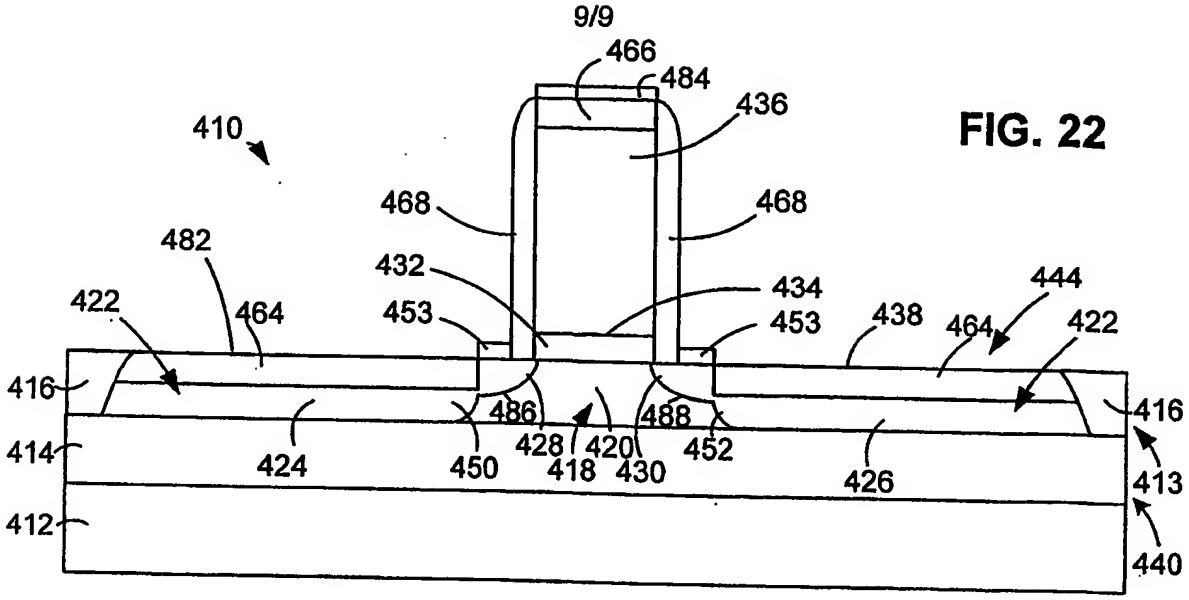
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FIG. 22

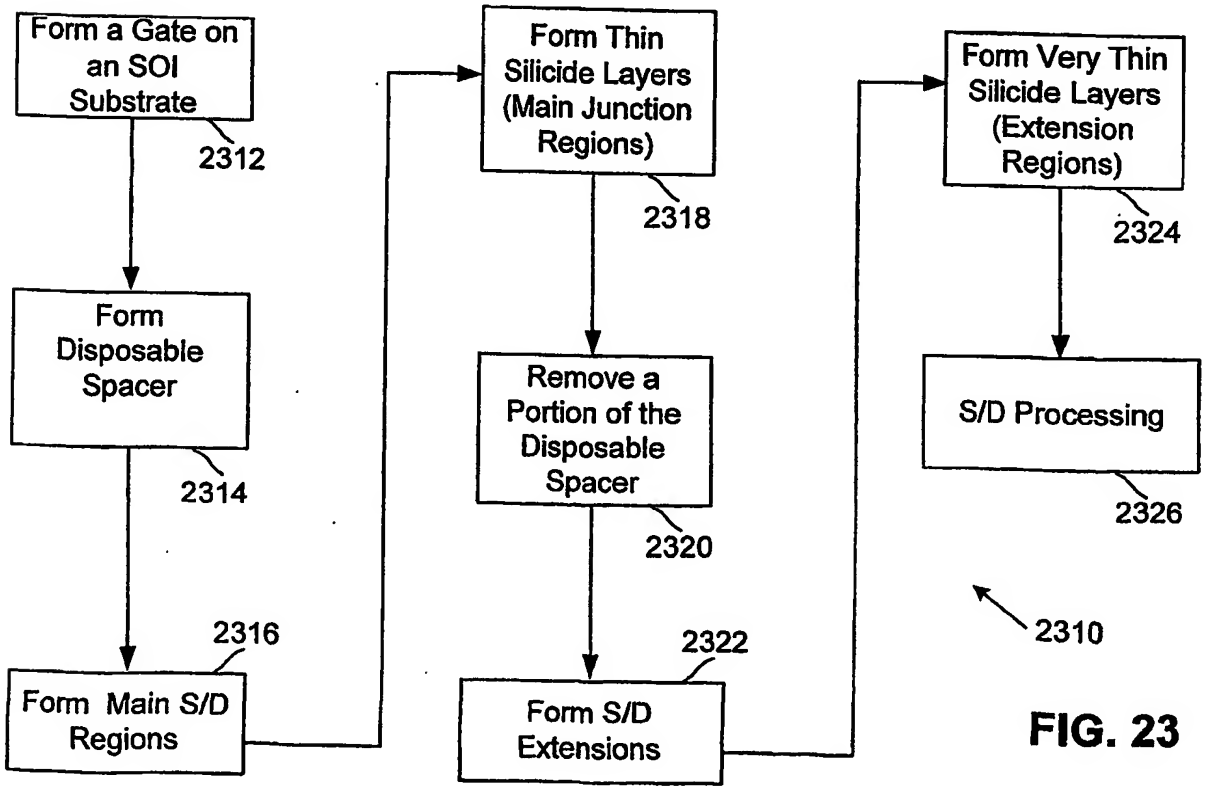
Form a Gate on an SOI Substrate
2312
Form Disposable Spacer
2314
2316
Form Main S/D Regions
Form Thin Silicide Layers (Main Junction Regions)
2318
Remove a Portion of the Disposable Spacer
2320
2322
Form S/D Extensions
Form Very Thin Silicide Layers (Extension Regions)
2324
S/D Processing
2326
2310

FIG. 23